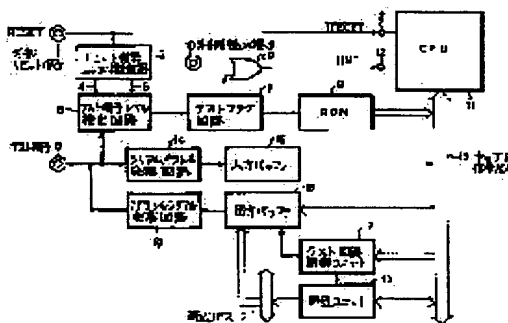


(11)Publication number : 05-036904
(43)Date of publication of application : 12.02.1993

H01L 27/04
G01R 31/318
H01L 21/66

(72)Inventor : HIRAYAMA TAKESHI

CONSTITUTION: A test flag circuit 7 is set by inputting a test terminal 8 at the time of falling of an external reset signal [external 1], and thus a CPU 11 starts a test circuit control unit 17 of a peripheral unit 13 on a chip by a ROM 9 which writes a test circuit starting procedure program. Setting of a condition at the time of testing and collection of data are conducted by a serial communication from the terminal 8 by using a serial/parallel converter 14 and a parallel/series converter 19.



[Date of extinction of right]